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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,224	12/22/2000	Walx Fang	4425-102	7196

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LOWE HAUPTMAN GILMAN & BERNER, LLP
1700 Diagonal Road, Suite 310
Alexandria, VA 22314

EXAMINER	
BARAN, MARY C	
ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/742,224	FANG ET AL.
	Examiner	Art Unit
	Mary Kate B Baran	2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The Examiner has reconsidered the finality of the rejection of the last Office Action. New art has been found and applied to the pending claims; therefore, the finality of that action is withdrawn.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Objections

4. Claims 1, 9, 17 and 19 are objected to because of the following informalities:

(a) In amended claim 1, page 8, line 3; amended claim 12, page 10, line 3; and amended claim 19, page 11, line 3; the language "plurality of integrate circuits" should be – plurality of integrated circuits –.

(b) In amended claim 9, page 9, line 2; the language "is adjusted to minimize the least squares" is unclear.

(c) In claim 17, page 16, lines 15-17; the language "wherein said simulating process is adjusted to let an error between said failure rate real time relation and said real time function is minimized" should be – wherein said simulating process is adjusted to minimize the difference between said failure rate test time relation and said testing time function –.

(d) In amended claim 19, page 12, "more than one said integrated circuits" should be – more than one of said integrated circuits –.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 11-15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyington et al. (U.S. Patent No. 6,377,897) (hereinafter Boyington) in view of Chien et al. ("A Nonparametric Approach to Estimate System Burn-in Time") (hereinafter Chien).

Referring to claims 1 and 12, Boyington discloses providing a plurality of integrated circuits (see Boyington, column 3 lines 31-33); performing a life-time testing process, wherein a failure rate testing time relation is established by measuring the life-time of each integrated circuit under a testing environment (see Boyington, column 4

lines 5-11), wherein an acceleration factor function (i.e. failure rate calculation) is related to the relationship between a testing time of the testing environment and a real time of a normal operating environment (see Boyington, column 3, lines 61-63 and column 4 lines 24-29); performing a transforming process using the acceleration factor function to transform the testing time function into a real time function (see Boyington, column 3 line 61 – column 4 line 4); a knee point of the real time function corresponds to an operation time which is a best burn-in time (see Boyington, column 3 line 61 – column 4 line 4 and column 4 lines 8-23); and performing an integrating process by integrating a real time function through a calculating region to acquire an accumulated failure rate real time function, wherein the calculating region is a region in which the real time is larger than the best burn-in time (see Boyington, column 3 lines 40-47). Boyington does not disclose simulating a failure rate testing time relation, or simulating a failure rate real time relation.

Chien discloses simulating a failure rate real time relation (page 463, "III. Methods" and "B. Simulation").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Boyington to include the teachings of Chien, because simulating a failure rate real time relation that was transformed from a failure rate testing time function allows the skilled artisan to calculate the reliability (i.e. total costs and the mean residual lives) under different burn-in times (see Chien, page 463, "III. Methods").

Referring to claims 2 and 13, Boyington discloses a failure rate testing time relation divided into three periods: infant mortality, normal, and wear out (see Boyington, Figure 3 and column 4 lines 5-8).

Referring to claims 3-8, 14 and 15, Boyington teaches all the features of the claimed invention except for a function (i.e. acceleration factor function) as constant, linear, or nonlinear; nor does Boyington disclose a testing time function that is an exponent function, a polynomial, or "$y=at^b$".

Chien discloses an acceleration factor function that is constant, linear, and nonlinear; and a testing time function that is an exponent function, a polynomial, and in the form "$y=at^b$" (i.e., Equation (1) and Equation (3), which depending on the values of variables λ and β (i.e., "a") and "D" (i.e., "b"), will represent an acceleration factor that is constant, linear, or nonlinear, and a testing time function that is exponential, polynomial, or "$y=at^b$" (see Chien, pages 462-463, "A. U-Shaped Failure Rate Function" and "A. Generating a U-Shaped Failure Rate Curve"), because failure rate is related to testing time and the acceleration factor function.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Boyington to include the teachings of Chien, because having an acceleration factor function that is constant, linear, and nonlinear; and a testing time function that is an exponent function, a polynomial, and "$y=at^b$" allows the skilled artisan to calculate the failure rate in various regions of the failure rate curve

including the constant failure rate region and the wear-out section (see Chien, page 463, "A. Generating a U-Shaped Failure Rate Curve").

Referring to claims 11 and 18, Boyington discloses all the features of the claimed invention except for stopping the integrating process when the testing time is located in the wear out period.

Chien discloses stopping the integrating process when the testing time is located in the wear out period.[i.e., "t_{L2}" is calculated (i.e., via an integration/summing process; page 463, A. Generating a U-Shaped Failure Rate Curve) to determine when the product starts to wear out (see Chien, page 463, "III. Methods")].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Boyington to include the teachings of Chien, because stopping the integrating process when the testing time is located in the wear out period would have allowed the skilled artisan to set a warranty plan and a construct a life-cycle model (see Chien, page 463, "III. Methods").

6. Claims 9, 10, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyington et al. (U.S. Patent No. 6,377,897) in view of Chien et al. and further in view of Tegethoff (U.S. Patent No. 5,539,652).

Referring to claims 9, 10, 16 and 17, Boyington teaches all the features of the claimed invention except for adjusting the simulation to minimize error using the least squares method.

Tegethoff teaches adjusting the simulation to minimize error using the least squares method (see Tegethoff, column 29 lines 27-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Boyington and Chien to include the teachings of Tegethoff, because minimizing the error allows the skilled artisan to enhance the reliability of the simulation.

7. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyington et al. (U.S. Patent No. 6,377,897) in view of Chien et al. and further in view of Matsuoka (U.S. Patent No. 5,204,618).

Referring to claim 19, Boyington discloses providing a plurality of integrated circuits (see Boyington, column 3 lines 31-33); performing a life-time testing process, wherein the life-time of each integrated circuit is measured under a testing environment (see Boyington, column 4 lines 5-11) and a failure rate testing time relation is established in accordance with a plurality of testing records (see Boyington, column 4 lines 24-29), wherein an acceleration factor function is related to the relationship between a testing time of the testing environment and a real time of a normal operating environment (see Boyington, column 3 line 61 – column 4 line 4 and column 4 lines 8-23), and performing an optimization process where part of the testing records are deleted and the process is performed again while more than one integrated circuit is failed (see Boyington, column 3 lines 16-29 and column 4 lines 24-29). The Examiner notes that Boyington does not explicitly delete records, but rather a subset of prior

records are used to optimize the determination of best burn-in time, which is functionally equivalent to the deletion of a portion of prior testing records/historical data.

Boyington further teaches performing a transforming process using the acceleration factor function to transform a specific testing time into a specific real time and transform a testing time polynomial into a real time polynomial (see Boyington, column 3 line 61 – column 4 line 4), wherein the specific real time corresponds to an operation time which is a best burn-in time for testing the integrated circuits (see Boyington, column 4 lines 8-23); and performing an integrating process by integrating a real time function through a calculating region to acquire an accumulated failure rate real time function (see Boyington, column 3 lines 40-47), wherein the calculating region is a region in which the real time is larger than the best burn-in time (see Boyington, column 4 lines 5-23). Boyington does not disclose simulating a failure rate testing time relation using a polynomial of the testing time; or determining a best testing time of the integrated circuits while only one of the integrated circuits has failed before a specific testing time.

Chien et al. discloses simulating a failure rate real time relation (see Chien, page 463, "III. Methods" and "B. Simulation").

Matsuoka discloses a monitored burn in system that has the capability of outputting an electrical signal when one of the integrated circuits fails, and calculating a cumulative failure rate, counting the cumulative number of failed integrated circuits at predetermined time intervals, and commanding burn-in to stop when a predetermined reference number of integrated circuits has failed (see Matsuoka, column 3 lines 10-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Boyington to include the teachings of Chien because simulating a failure rate real time relation that was transformed from a failure rate testing time function allows the skilled artisan to calculate the total costs and the mean residual lives under different burn-in times (see Chien, page 463, "III. Methods"). It would further have been obvious to one of ordinary skill in the art to modify Boyington and Chien to include the teachings of Matsuoka because monitoring the burn-in process and stopping the procedure when a predetermined number of ICs have failed, would have allowed the skilled artisan to enhance the reliability of the burn-in procedures (see Matsuoka, column 1 lines 21-28).

Referring to claim 20, Boyington and Matsuoka teach all the features of the claimed invention except for stopping the integrating process when the testing time is located in the wear out period.

Chien discloses stopping the integrating process when the testing time is located in the wear out period.[i.e., "t_{L2}" is calculated (i.e., via an integration/summing process; (page 463, A. Generating a U-Shaped Failure Rate Curve) to determine when the product starts to wear out (see Chien, page 463, "III. Methods")].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Boyington and Matsuoka to include the teachings of Chien, because stopping the integrating process when the testing time is located in the

wear out period allows the skilled artisan to set a warranty plan and a construct a life-cycle model (see Chien, page 463, "III. Methods").

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B Baran whose telephone number is (703) 305-4474. The examiner can normally be reached on Monday - Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (703) 308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

MKB
February 20, 2003

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800